

Power MOSFET “SuperFAP-G Series” for Low-Loss, High-Speed Switching

Tadanori Yamada
Atsushi Kurosaki
Hitoshi Abe

1. Introduction

With the progress of our high-level information based society, personal computers, mobile internet terminals, and BS digital TVs have rapidly become popular among consumer households. Preparation and innovation have also progressed for the internet server and high-speed backbone network infrastructures which support these information services. For these reasons, electric energy consumption has increased by 2.2 to 3.0% a year on average. There is concern that this increase may be a cause of global warming. Therefore, the International Energy Star Program started in 1995 for the purpose of reducing the stand-by electric consumption of office automation machines, at which they operate for long periods of time. Furthermore, electric utility industries and companies have struggled to obey the Revised Energy Saving Law and to implement energy conservation measures of the “first runner method” established by COP3 (The 3rd Session of the Conference of the Parties: Prevention of Global Warming Meeting in Kyoto) in 1997.

The subjects for energy conservation are consumer electronics devices such as air conditioners, TVs, lighting and office automation machines such as computers, display monitors and printers. The power conversion units for these types of equipment use characteristically high-efficiency switched mode power supply (SMPS). But, reflecting the trend toward energy conservation, there are increasing demands for such power supplies with higher efficiency, lower loss and reduced stand-by waiting power.

This paper presents a summary of the characteristics of the new “SuperFAP-G” series of power MOSFETs developed based on market trends for low loss, super high speed switching.

2. Required Specifications for Power MOSFETs

Figure 1 through Figure 3 show the typical 3 types of simulation results for the power loss in an SMPS.

The ringing choke converter has characteristics such as a varying switching frequency that changes depending on the output power. At light loads, the

Fig.1 Power loss simulation result of ringing choke converter

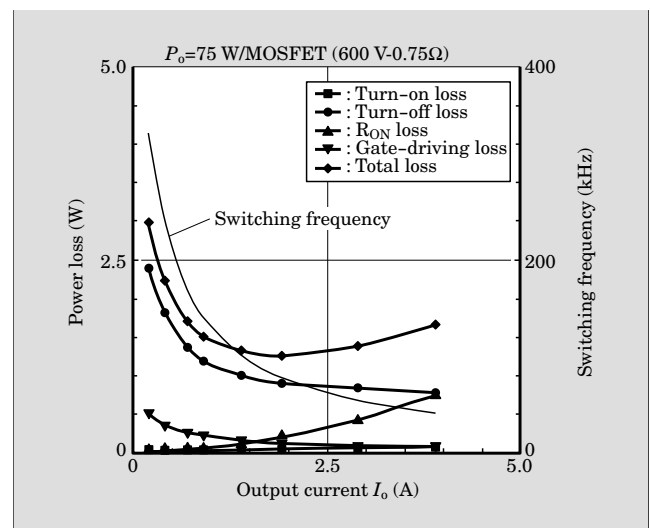
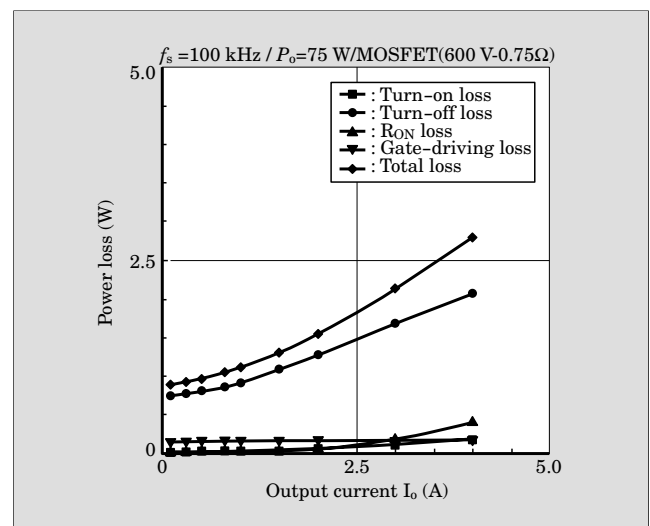
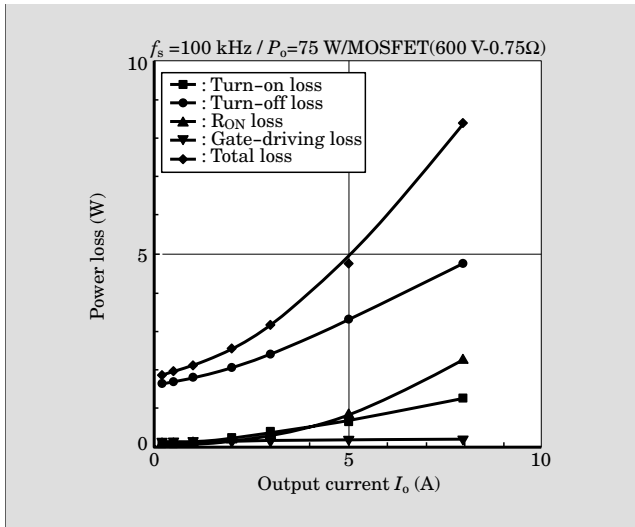


Fig.2 Power loss simulation result of flyback converter



switching frequency increases to more than 300kHz. For that reason, losses due to turn-off and gate driving account for about 80% and 18% of total loss respectively in the light load mode. In the rated load mode (output current: 3.9A), switching frequency decrease to less than 100kHz and on-state loss $R_{DS(on)}$ becomes the

Fig.3 Power loss simulation result of forward converter



same as turn-off loss due to the higher on-duty.

The external fly back converter differs from the self-oscillated ringing choke converter and fixes the switching frequency at the optimum controllable value. The turn-off loss accounts for about 83% of the total loss in the light load mode and 74% in the rated load mode (output current: 3.9A). The percentage of turn-off loss accounts for the majority of loss in the full-load mode.

The switching frequency of the forward converter is also fixed similarly to that of the external fly-back converter. About 90% of the total loss is turn-off loss in the light load mode. At the rated load (output current: 8A), turn-off loss occupies about 50% of the total loss. The rate of on-state resistance loss also increases with the increasing output current and at the rated load mode, reaches about 32% of total loss.

The following can be observed from the loss simulation results of each type of converter. The 3 items below are important characteristics required by power MOSFETs in order to reduce stand-by and SMPS power loss.

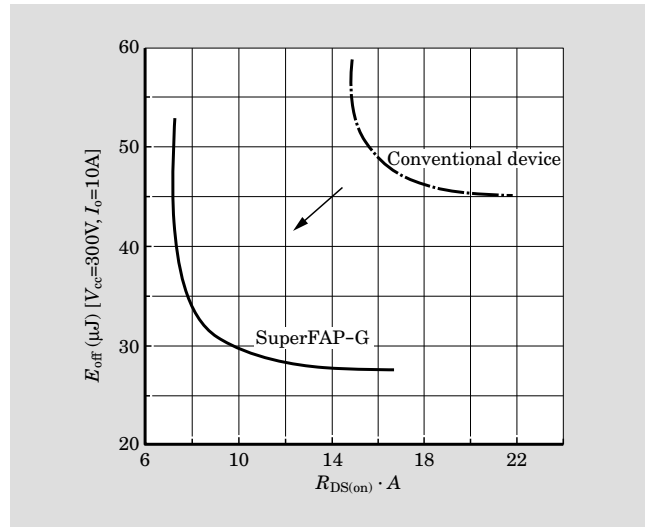
- (1) Reduction of turn-off loss
- (2) Reduction of $R_{DS(on)}$ loss
- (3) Reduction of gate driving loss

The switching frequency in loss simulation is the result from analysis using the switching frequency of a general SMPS. Future technology is expected to increase the switching frequency even more in order to minimize the size of SMPS. In such a case, reducing the turn-off and gate driving losses will become even more important.

3. Design Technologies

As described above, the main requirement for switching regulator power supplies is reduced loss at turn-off and $R_{DS(on)}$. However, there is a trade-off involved in both types of loss. It is important to

Fig.4 $E_{off} - R_{DS(on)}$ trade-off characteristics



improve the trade-off relation to reduce both $R_{DS(on)}$ and turn-off losses.

Figure 4 shows the improved trade-off characteristics of turn-off loss versus on-state resistance for the new “SuperFAP-G” series of power MOSFETs.

By combining three newly developed technologies, the “SuperFAP-G” series has reduced by half the typical turn-off loss at the same on-state resistance characteristic. This paper describes specifically the design policy which realized the improved trade-off relation.

3.1 Low $R_{DS(on)}$ technology

Over 90% of the on-state resistance characteristics of 500V and above high-voltage power MOSFETs are determined largely by the resistivity of the epitaxial layer. Therefore it is possible to reduce the epitaxial layer’s resistance to achieve low on-state resistivity, but this method has the drawback of decreasing the drain-source breakdown voltage V_b .

Figure 5 - ① shows V_b versus $R_{on} \cdot A$ characteristics of the conventional polygonal cellular structure with high electric-field of the cellular part due to use of a high resistance epitaxial layer.

We applied stripe-shaped cellular structures to the “SuperFAP-G” series to lessen the high electric field in the structures as shown in Fig. 6.

By applying fine patterning technology in a precision alignment process, the electric field in the cellular part is lessened by reducing the width of the surface drain layer and optimizing the depth, width and doping profile of the p-well.

With this design, the cellular part maintains its breakdown voltage. Therefore, the lower resistivity of the epitaxial layer can be applied to the MOSFET.

3.2 Optimized guard-ring technology

We have established a design which lessens the electric field of cellular structures through utilization

Fig.5 On resistance $R_{on} \cdot A$ versus breakdown voltage V_b

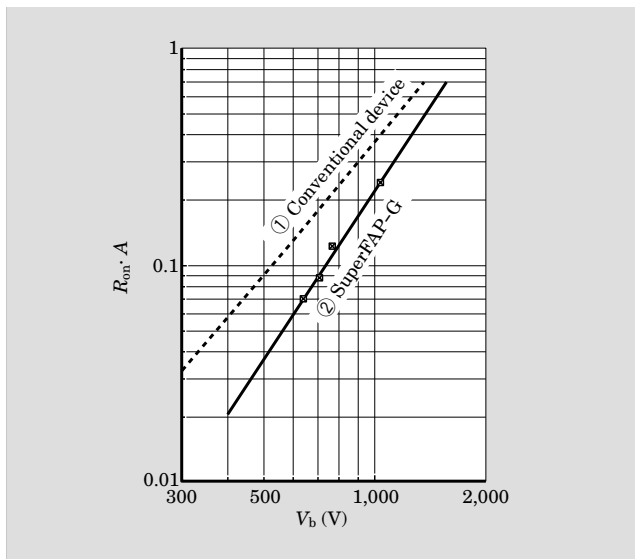
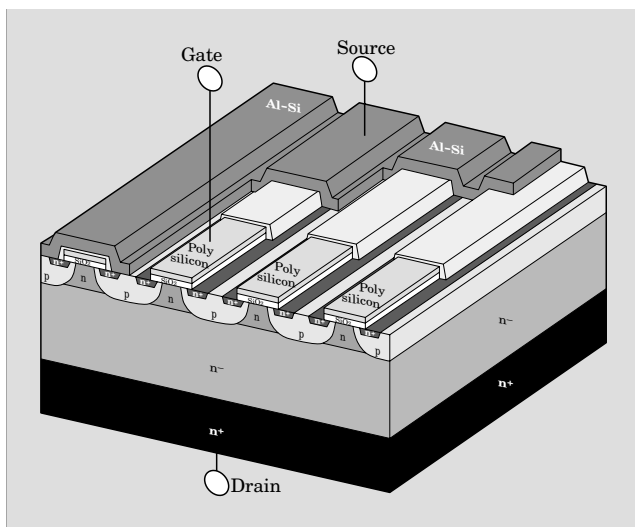


Fig.6 Stripe-shaped cellular structure of SuperFAP-G

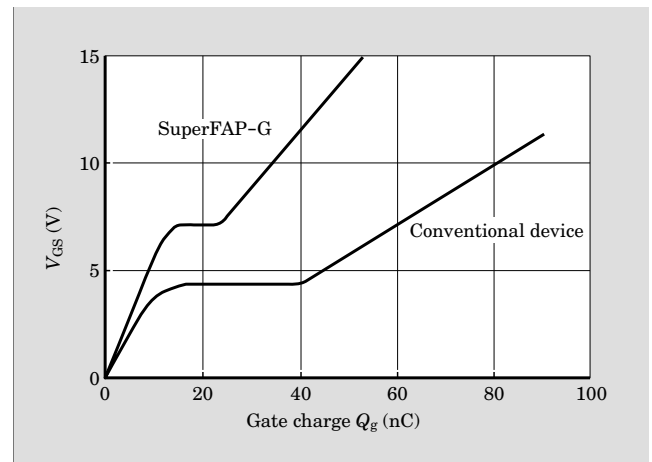


of the lower resistivity of an epitaxial layer. But, there are some problems of unbalance in which the breakdown voltage decreases between cellular regions, due to the increased electric field of the conventional guard-ring design technology.

Newly developed inequality pitched optimized guard-ring (OGR) technology has been applied to this device, in order to lessen the breakdown voltage at the guard-ring field of the low resistance epitaxial layer.

We have designed the optimum pitch, width and spacing for each guard ring and number of guard rings by simulating the electric field of these cellular structures to decrease the field. By integrating the above described design of cellular stripe-shaped structures and OGR structures, a MOSFET with higher breakdown voltage can be realized through utilization of the low resistance epitaxial layer.

Fig.7 Gate charge characteristics (600V-0.75Ω device)



As shown in Fig. 5 - ②, the relation of $R_{on} \cdot A$ versus drain-source breakdown voltage V_b is improved, and on-state resistivity has been reduced by half compared to conventional devices.

3.3 Low gate-drain charge (Q_{gd}) technology

In order to reduce the turn-off power loss, which is determined by the charge time constant of drain-gate miller capacitance C_{rss} , it is necessary to decrease the gate-drain charge Q_{gd} .

As $R_{DS(on)}$ and Q_{gd} have a trade-off relation, J-FET resistance can be reduced by designing cells with larger gate poly-silicon areas. However, unfortunately Q_{gd} increases with increasing C_{rss} .

In order to improve the trade-off relation of the “SuperFAP-G” series, we have designed the cellular part with a smaller gate electrode area using the poly-silicon precision alignment process of fine patterning technology. Meanwhile, the design restricts the increase in J-FET resistance by optimizing the profile of the n-type doping impurity.

As the result of the above cell design, a Q_{gd} characteristic was realized that is lower than the Q_{gd} of conventional devices by about 1/3.

Figure 7 compares gate charge characteristics at the same on-state resistance.

4. Characteristics

Table 1 shows a typical model of the recently developed “SuperFAP-G” series. We have defined a FOM (figure of merit) which indicates the MOSFET power loss as the product of on-state resistivity and gate-drain charge Q_{gd} .

The typical FOM of this recently developed model was $5.75\Omega \cdot nC$, which is approximately 3 times the FOM value of conventional devices at the same on-state resistance.

A product line of this series is planned with breakdown voltages in the 450V to 900V class.

Table 1 Ratings

Item	2SK3450-01	2SK3504-01
V_{DS}	600V	500V
I_D	$\pm 12A$	$\pm 14A$
P_D	115W	115W
$V_{GS(th)}$	3 to 5V	3 to 5V
$R_{DS(on)}$	0.65 Ω max	0.46 Ω max
Q_g	34nC	33nC
Q_{gs}	12.5nC	12.5nC
Q_{gd}	11.5nC	10.5nC
FOM $R_{on} \cdot Q_{gd}$	5.75 $\Omega \cdot nC$	3.68 $\Omega \cdot nC$

Table 2 Operating result of commercial SMPS (forward converter)

(a) Standby mode ($P_o = 2W$, $f_c = 130kHz$)

Type	Item	Conversion efficiency η_{DC-DC}	MOSFET loss P_{loss}	MOSFET temperature rise ΔT_c
Conventional device 600V/0.75 Ω / TO-3PF		31.90%	1.28W	5.8 $^{\circ}C$
SuperFAP-G 600V/0.75 Ω / TO-220F		35.10%	0.82W	2.6 $^{\circ}C$

(b) Rated load mode ($P_o = 125W$, $f_c = 130kHz$)

Type	Item	Conversion efficiency η_{DC-DC}	MOSFET loss P_{loss}	MOSFET temperature rise ΔT_c
Conventional device 600V/0.75 Ω / TO-3PF		81.40%	8.31W	54.0 $^{\circ}C$
SuperFAP-G 600V/0.75 Ω / TO-220F		83.30%	4.47W	34.1 $^{\circ}C$

5. Application to the SMPS

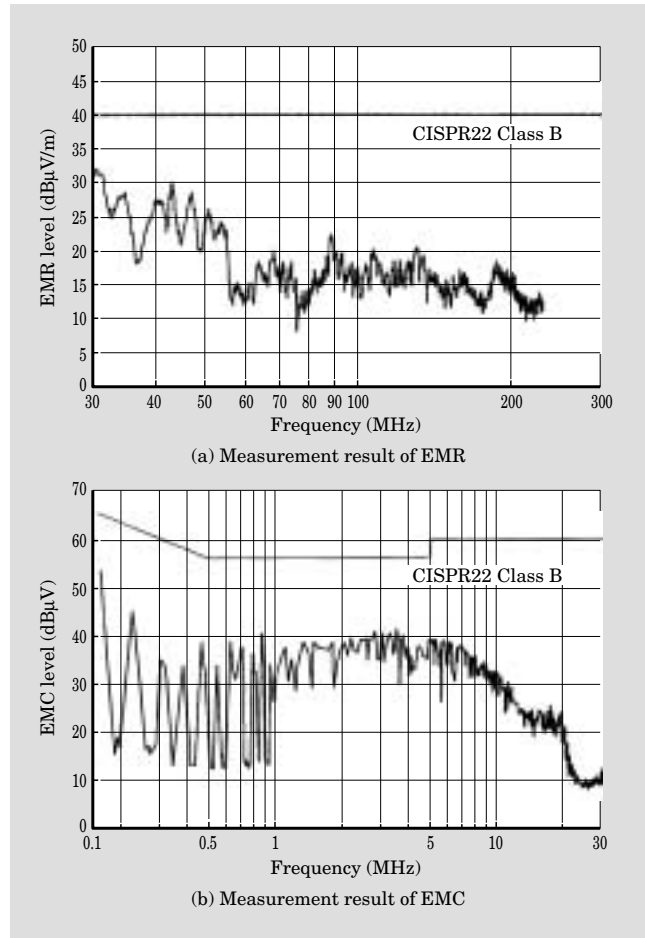
As a reference example, Table 2 shows the results (reference values) of applying the newly developed “SuperFAP-G” series to a forward converter SMPS.

The power MOSFET loss decreased by 35% and the conversion efficiency improved by 3.2% compared with a conventional device in the stand-by mode.

In spite of the smaller package than that of conventional devices, the heat sink can be miniaturized due to the low temperature rise of 20 $^{\circ}C$ at the rated load. Compared to conventional devices at the same temperature rise, output will increase by about 20%.

Figure 8 shows the EMI measurement results

Fig.8 EMI measurement result



(reference) when a “SuperFAP-G” series device is used in the AC adapter of a commercial fly-back converter. In the case of lower Q_{gd} , in another words higher-speed switching, EMC noise is at the same level as in a conventional device and EMR noise is approximately +2dB at peak. Therefore, the “SuperFAP-G” series satisfies the CISPR Pub.22 Class B standard.

6. Conclusion

This paper has presented the developed technology and a product summary of Fuji Electric’s newly developed “SuperFAP-G” series of low loss, high-speed switching power MOSFETs.

We at Fuji Electric, believe that the “SuperFAP-G” series will contribute to society with its higher efficiency, lower stand-by loss, increased output power density and smaller size.

At the same time, based on the same technology, we are planning to develop a series of medium voltage power MOSFETs of 100 to 250V for application to higher frequency switching DC-DC converters.